

April 9, 2004

To: Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

 $\overline{\text{Serial No.}}$ 10/772,939 02/05/04

Liang-Gi Yao et al.

A NOVEL DEPOSITION METHOD FOR Si-Ge EPI LAYER ON DIFFERENT INTERMEDIATE SUBSTRATES

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 1° , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Signature/Date

TSMC-02-029

- U.S. Patent 6,388,307 to Kondo et al., "Bipolar Transistor," describes a B-doped SiGe layer in a transistor process.
- U.S. Patent 5,976,941 to Boles et al., "Ultrahigh Vacuum Deposition of Silicon (Si-Ge) on HMIC Substrates," describes a SiGe epi process.
- U.S. Patent 5,273,930 to Steele et al., "Method of Forming a Non-Selective Silicon-Germanium Epitaxial Film," describes a SiGe epi process on a silicon seed layer.
- U.S. Patent 5,620,907 to Jalali-Farahani et al., "Method for Making a Heterojunction Bipolar Transistor," describes a method for a heterojunction bipolar transistor.

Sincerely

Stephen B. Ackerman,

Reg. No. 37761

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